

ZC3 BLOCK DIAGRAM

AMD K8/RX485/SB460 REV:B

BOM
VRAM@ -> (Samsung, Infineon, Hynix)
UC@ -> (ATMEL, SST)
MEMID@ -> (Samsung, Infineon, Hynix)
2@ -> Add second source

SYSTEM POWER
MAX1999
Page 44

CPU CORE(MAX8774)
Page 41

+1.2V/+1.5V/+2.5V
Page 42

+1.8V / VGA_CORE
Page 43, 46

DISCHARGE CIRCUIT
Page 44

Clock GEN
ICS951462
Page 2

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
PCI 33MHz
REF 14MHz

R,G,B

CRT port
Page 26

LCD

LCD CONN
Page 25

TV-OUT

S-VIDEO
Page 25

TMDS

HDMI
Page 34

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
TI 7412	AD25	REQ0# / GNT0#	INTE#_F#_G#	PCICLK2
BCM5788M	AD20	REQ2# / GNT2#	INT#	PCICLK5

CPU THERMAL SENSOR
Page 13

AMD S1
Turion 64
(638 S1g1 socket)
Page 3, 4, 5, 6

DDR II
533,667MHz

DDR II-SODIMM1
Page 7, 8

DDR II-SODIMM2
Page 7, 8

HyperTransport I/O BUS
LINK 16X16

NORTH BRIDGE
RX485
465 FCBGA
Page 9, 10, 11, 12

PCIE 16X

ATI
M56-P
Page 18, 19, 20, 21, 22, 24

VRAM X4
(GDDR3 500MHz)
Page 23

2X PCI-E 0,1

1X PCI-E 3

1X PCI-E 2

USB 2.0 * 1(USB5)

A-LINK

PCI/33MHz

Azalia

DOCKING PORT
Page 32

Mini Card/WLAN
Page 29

New Card
Page 33

USB PORT X4
Page 29

BLUETOOTH
Page 29

1.3M Camera Module
Page 25

USB0: M/B IO
USB1: M/B IO
USB2: D/B IO
USB3: D/B IO
USB4:
USB5: NEW CARD
USB6: BLUETOOTH
USB7: CAMERA

SOUTH BRIDGE
SB460
549 BGA
Page 14, 15, 16, 17

Primary IDE HDD
Page 35

SATA

Media bay CDROM
Page 35

ATA 66/100

LPC/33MHz

RTC Battery
Page 14

SUPER I/O
PC87383
Page 38

Embedded Controller
NS 551
Page 39

FIR
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BIOS
Page 39

Keyboard
Page 40

Touchpad
Page 40

SWITCH & LED
Page 40

FAN
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AUDIO CODEC
ALC883
Page 36

HP AMP
Page 37

SPK AMP
Page 37

HP/ SPDIF
Page 37

INT SPK
Page 37

Line-in & MIC
Page 37

MDC1.5 MODEM
Page 36

RJ11
Page 45

CARDBUS/1394/Card reader
TI 7412
Page 30, 31

PCMCIA
Page 31

1394
Page 30

6 in 1 Cardreader
Page 31

Giga LAN
Broadcom
BCM5788MG
Page 27

RJ45
Page 28

EZ4 Docking Connector
Page 32

PCIe1~2 , Lan
Ser & Par Port
PS2 , VGA, DVI
SPDIF, SM BUS

PCI-Express X 2

TV out / CRT

Switch
Page 25, 26

Audio

Switch
Page 37

DVI

Switch
Page 34

10/100/1G

Switch
Page 28



PROCESSOR HYPERTRANSPORT INTERFACE

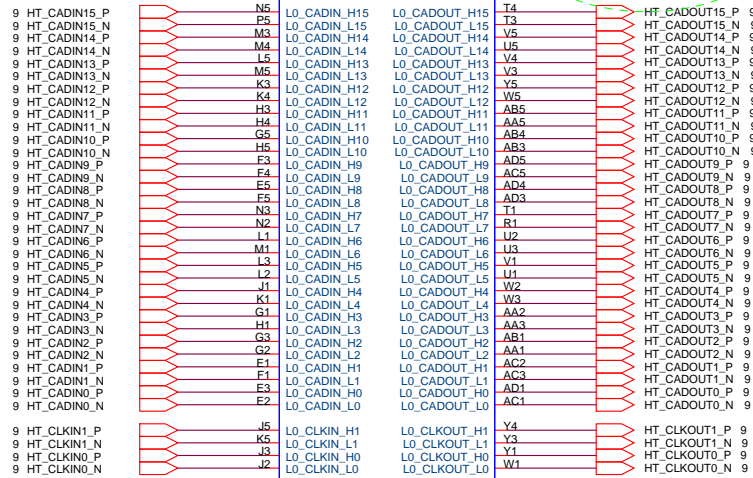
VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VLDT_RUN U43A

D4 VLDT_A3
D3 VLDT_A2
D2 VLDT_A1
D1 VLDT_A0

VLDT_B3
VLDT_B2
VLDT_B1
VLDT_B0

C495
4.7U/6.3V_6



VLDT_RUN

R274 49.9/F_4
R272 49.9/F_4

HT_CTLIN1_P
HT_CTLIN1_N
HT_CTLIN0_P
HT_CTLIN0_N

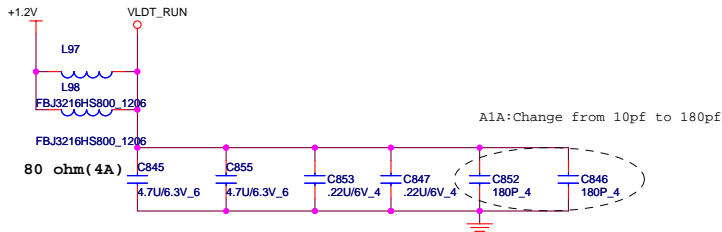
P3 HT_CTLIN1_P
P4 HT_CTLIN1_N
P1 HT_CTLIN0_P
HT_CTLIN0_N

L0_CTLIN_H1
L0_CTLIN_L1
L0_CTLIN_H0
L0_CTLIN_L0

L0_CTLOUT_H1
L0_CTLOUT_L1
L0_CTLOUT_H0
L0_CTLOUT_L0

HT_CPU_CTLOUT1_P
HT_CPU_CTLOUT1_N
HT_CTLOUT0_P
HT_CTLOUT0_N

T5
R5
R2
R3



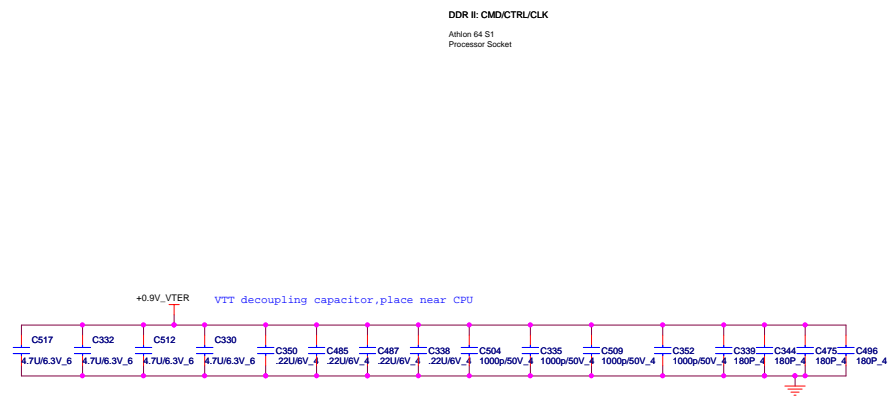
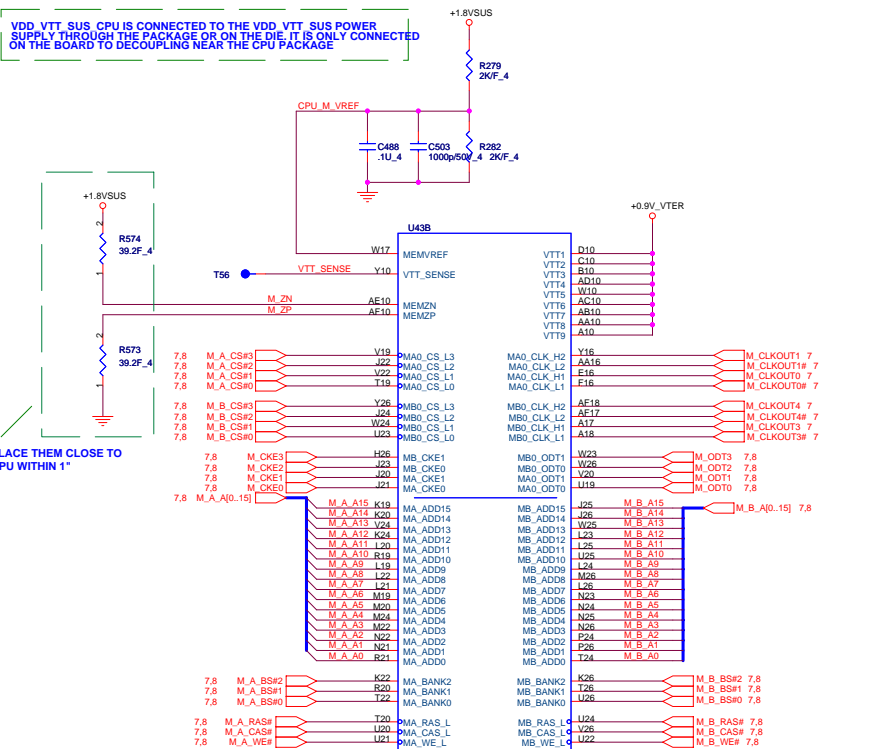
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

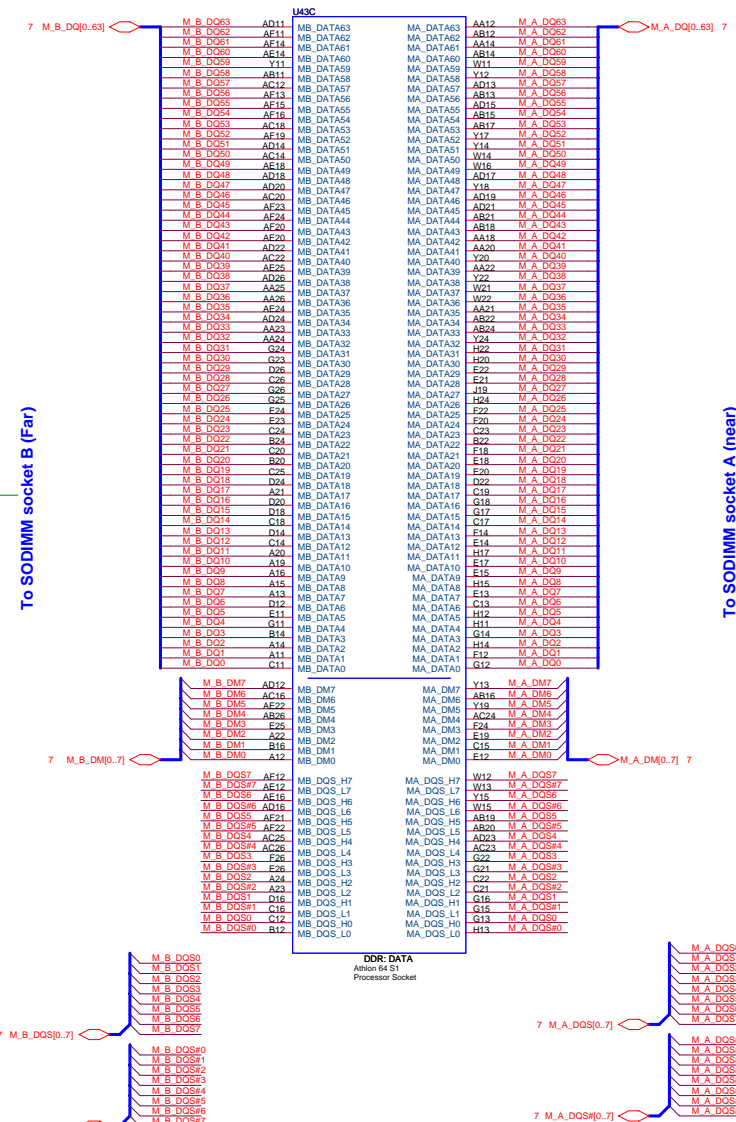


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Size	Document Number	Rev
	ATHLON64 HT V/F	1A
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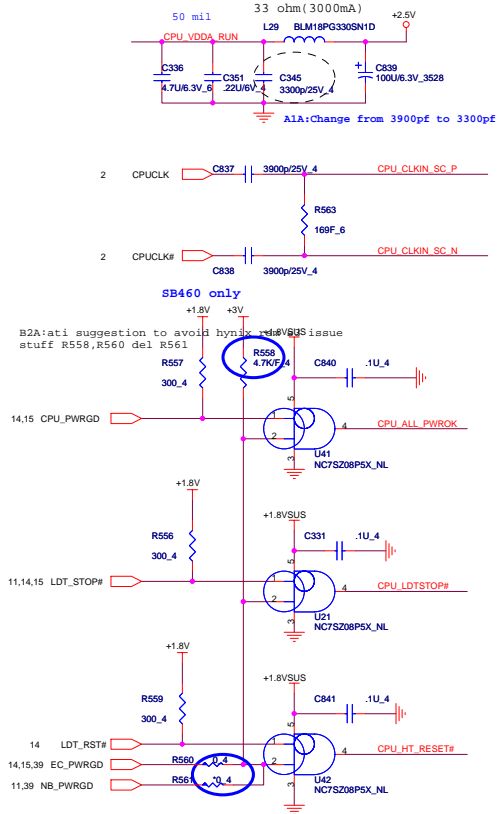
Processor DDR2 Memory Interface





LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

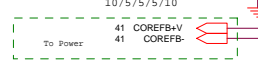
CPU_VDDA_RUN



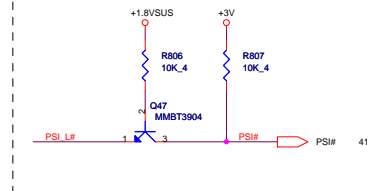
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pull-down to VSS.



place them to CPU within 1"

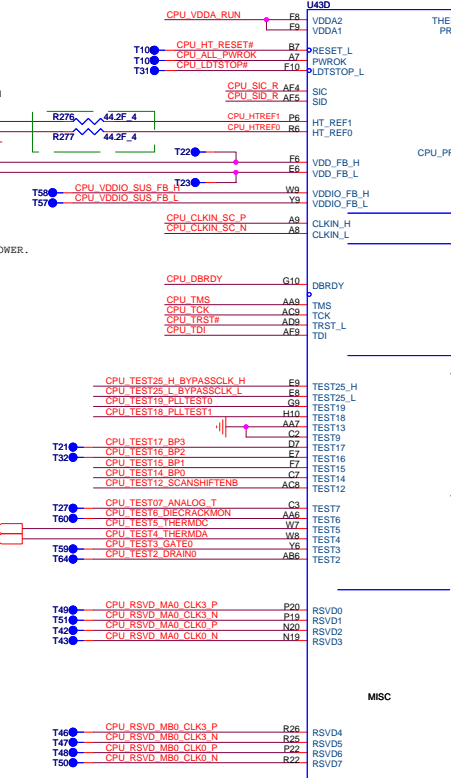


B2A: Add LEVEL-SHIFT circuit (R806, R807, Q47) on PSI# that between CPU and POWER.

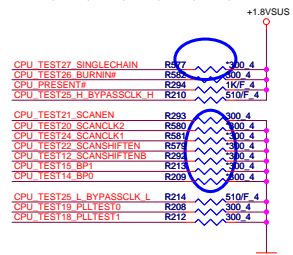


13 CPU_TESTS_THERMOC

13 CPU_TEST4_THERMDA



B2A: AMD suggestion not stuff R577, R580, R581, R579, R292, R213, R209



IF no use which Net need pull-up or down

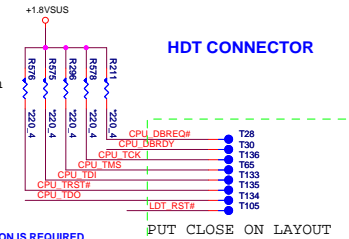
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.



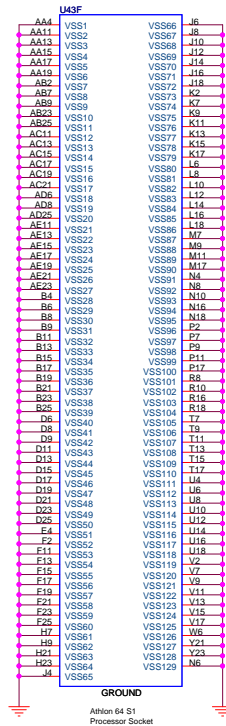
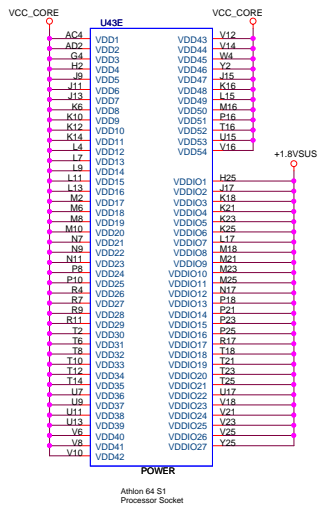
Power Status Indicator for the VDD Power Supply regulator. This signal may be used by the regulator to improve efficiency when the processor is in low power states.

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

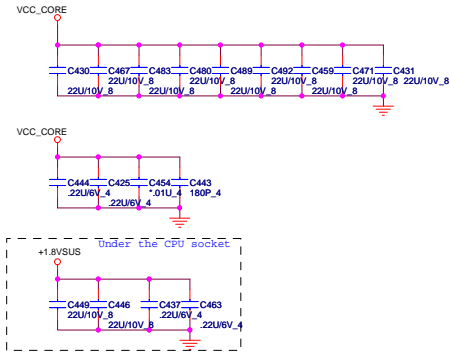
HDT CONNECTOR



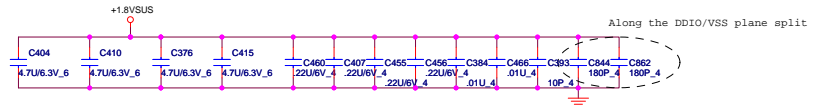
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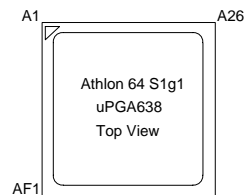
BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE

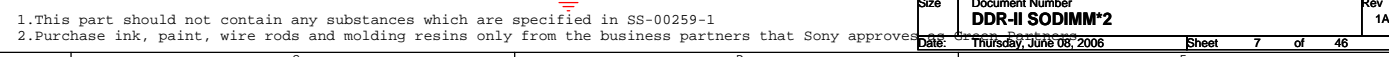


PROCESSOR POWER AND GROUND

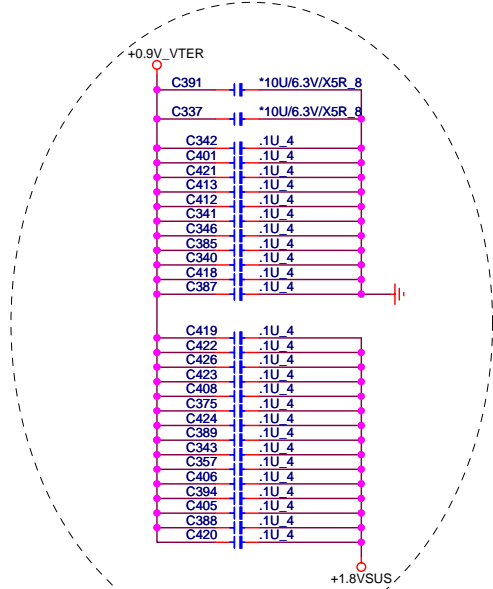


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Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
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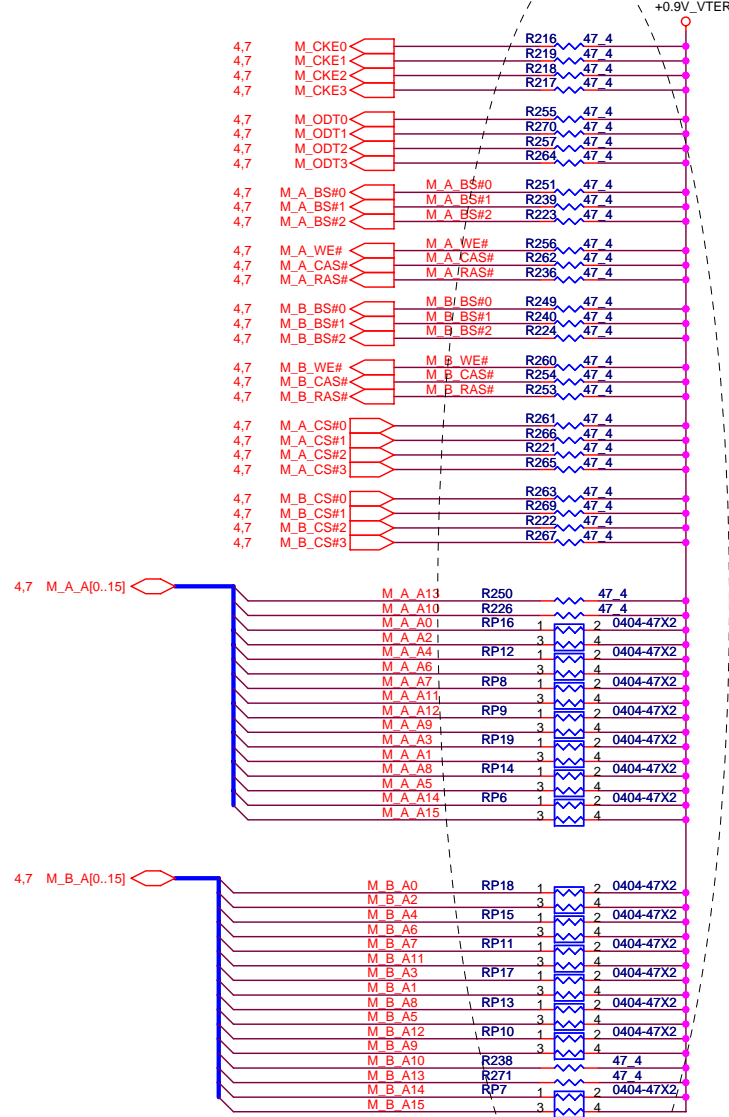


VTT is decoupled to VDDIO, VTT is decoupled to VSS



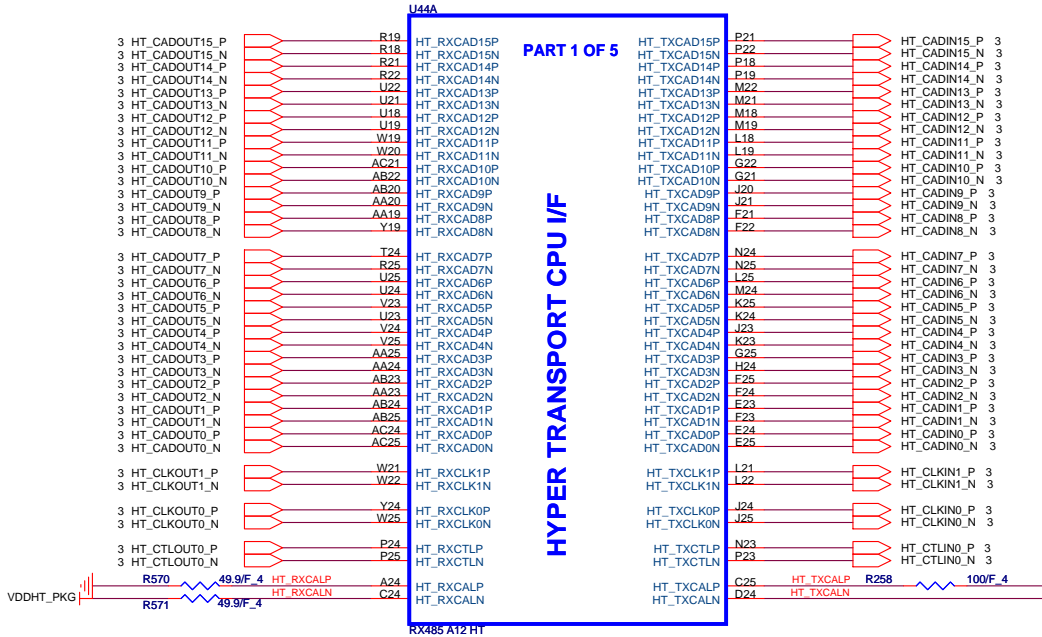
decoupling capacitors from VTT (+0.9V_VTER) to VDDIO (+1.8VSUS). Which is (1) decoupling capacitor for every (4) signals terminated to VTT

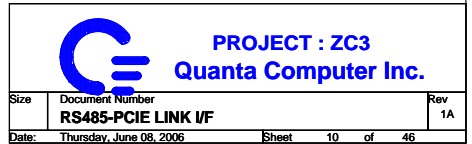
AlA:Change RTT termination from 56 to 47 ohm

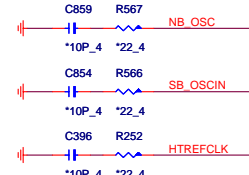
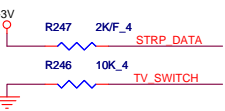
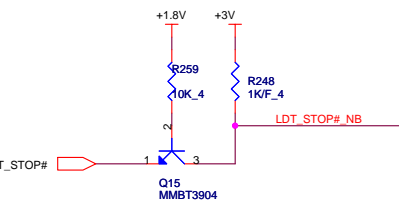
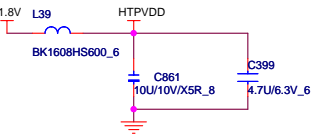
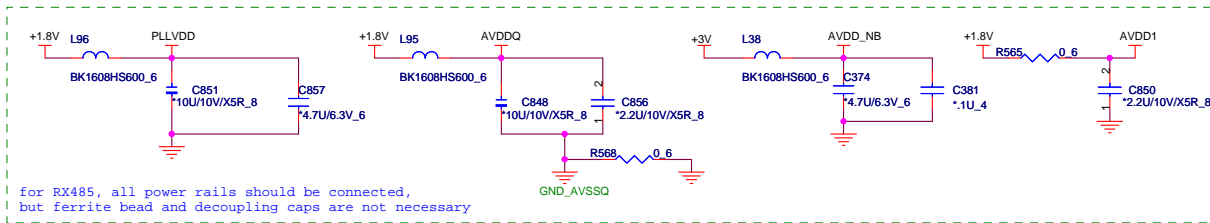


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Size	Document Number	Rev
	DDR-II TERMINATION	1A
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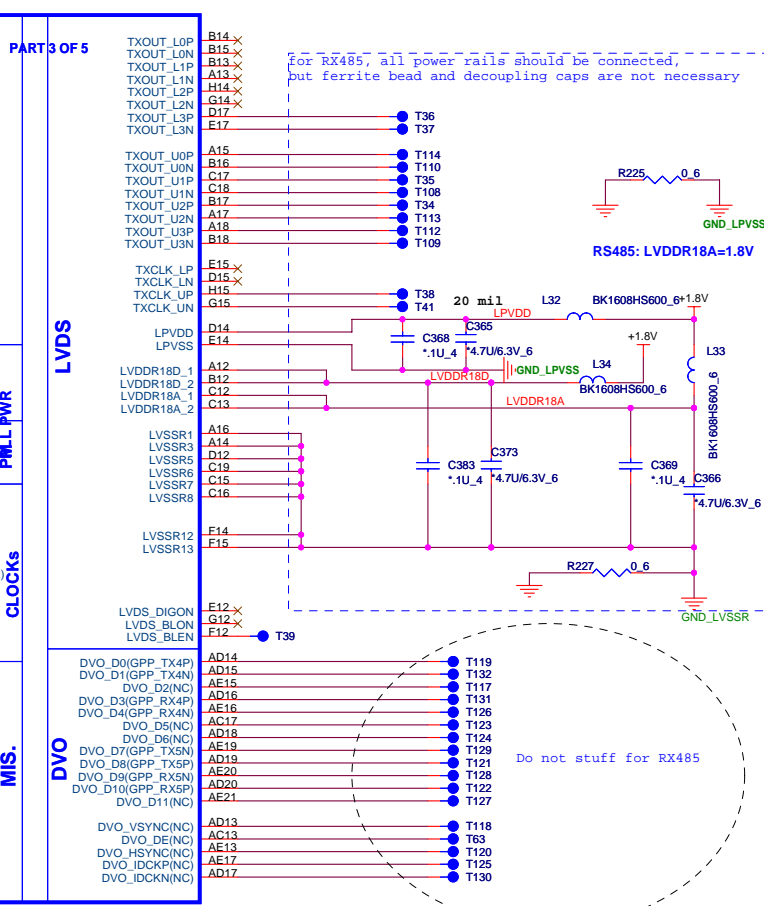
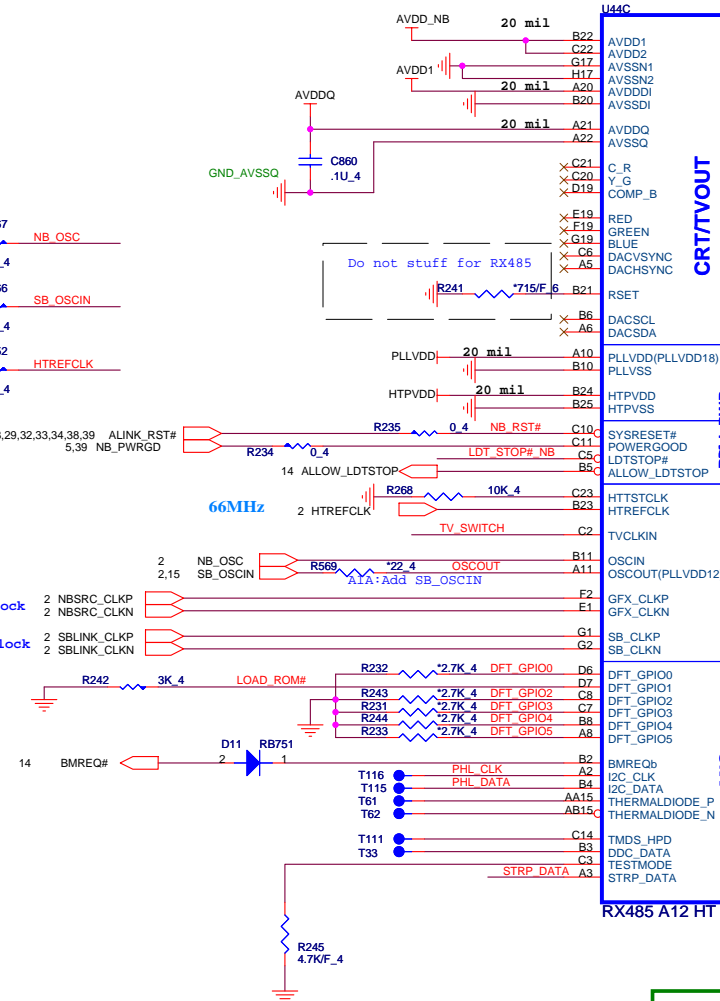






PCI-E graphic clock
A-Link clock

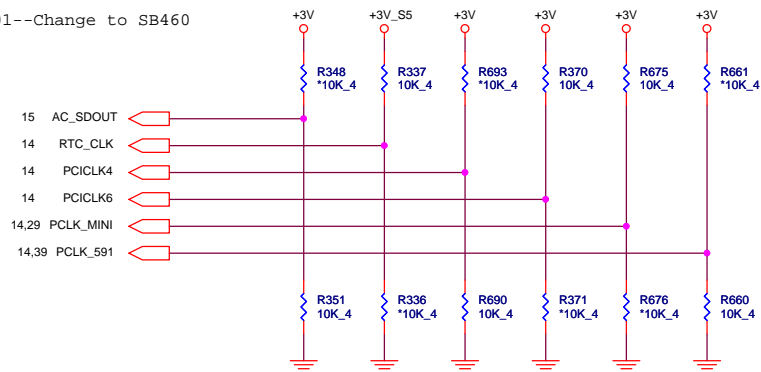
LOAD_ROM#: LOAD ROM STRAP ENABLE
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



RX485 A12 HT

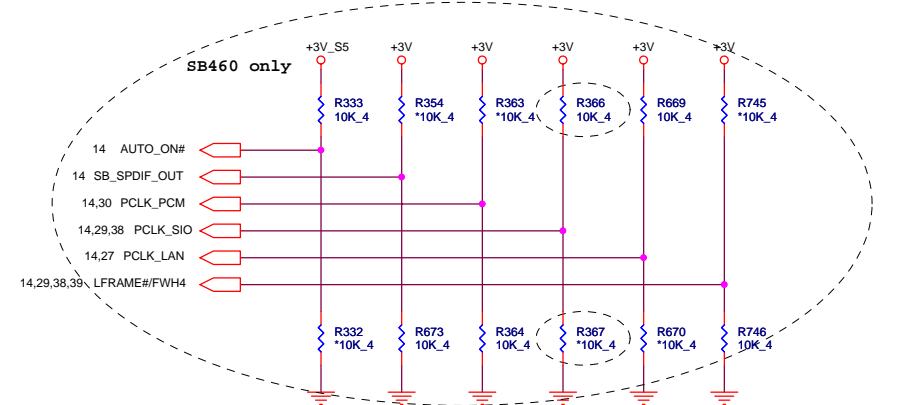
	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

Edison-11/01--Change to SB460



REQUIRED STRAPS

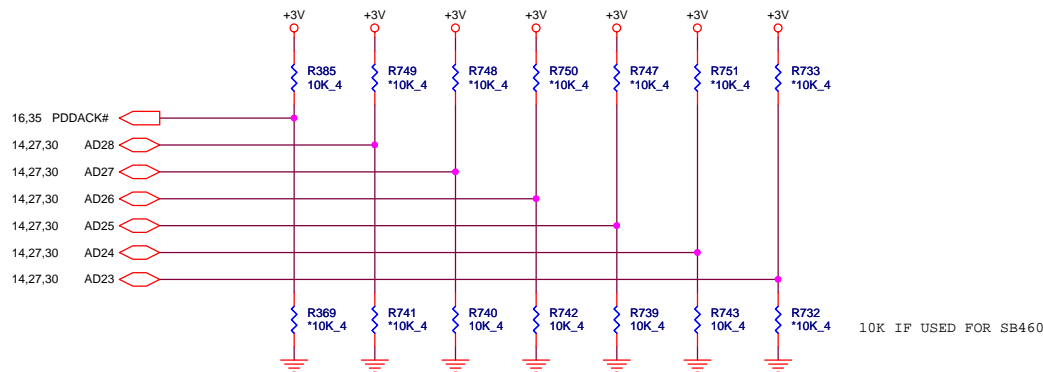
					PCLK_MINI	PCLK_591
					PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	DEFAULT



A1A:USB PHY POWERDOWN DISABLE

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE	PCIE_CM_SET LOW	ENABLE THERMTRIP#
PULL LOW	AUTO PWR ON	SIO 48MHz	48MHZ OSC MODE	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#


BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	

SB460 only SB600 only

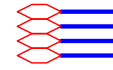
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Size Custom	Document Number	Rev 1A
SB460M STRAPS		
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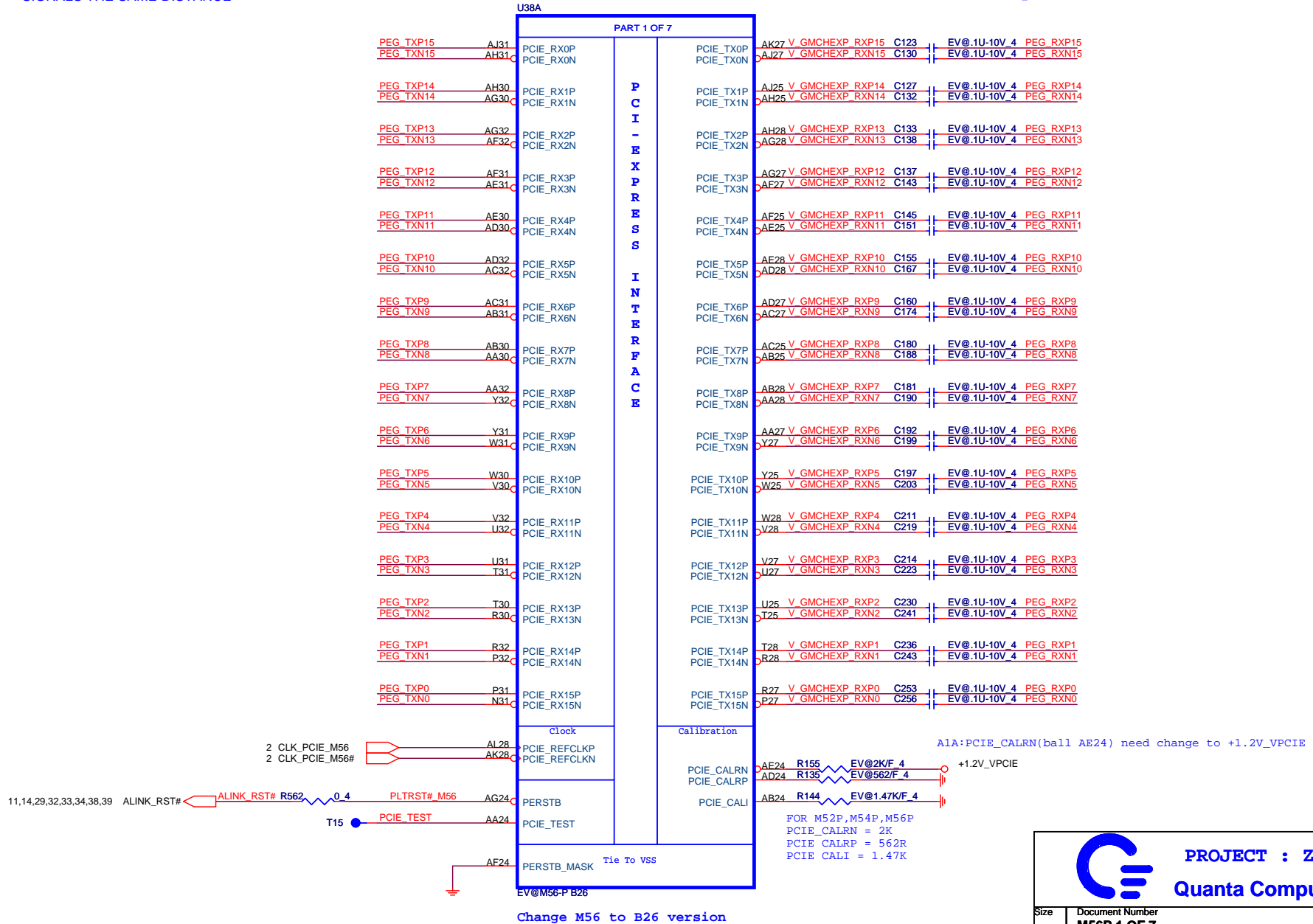
SB-4

PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

10 PEG_RXP[15:0]
10 PEG_RXN[15:0]
10 PEG_TXP[15:0]
10 PEG_TXN[15:0]



A1A:PCI-E 16X LAN are Swap



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	M56P 1 OF 7	1A
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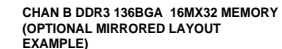
Channel B



-DQMS[0.7] 22
RDQSB[0.7] 22
WDQSB[0.7] 22

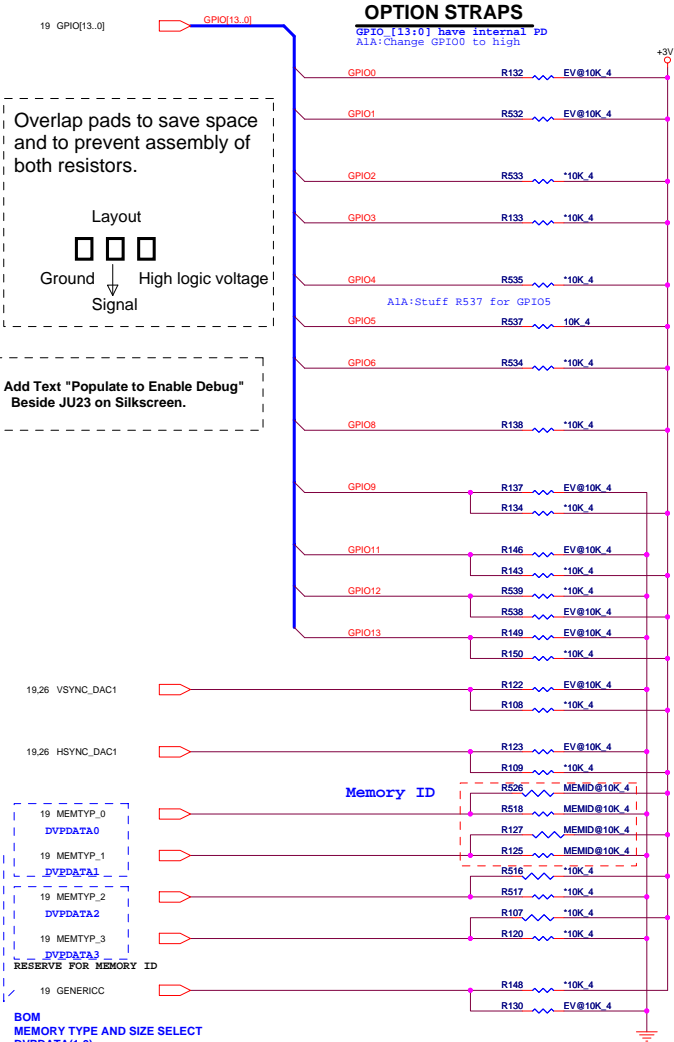
C3A:change footprint form c0
c0402

C3A:change footprint form c0402-c to c0402

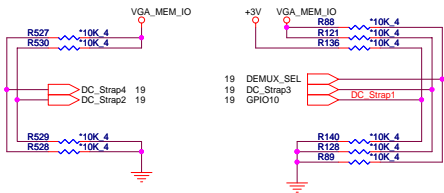


BOM

AKD5FW-T513	SAMSUNG GDDR3 (512M
AKD5FWBT*00	Infineon GDDR3(512M



BOM
MEMORY TYPE AND SIZE SELECT
DVPDATA(1:0)
00 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package
01 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package
10 - Hynix GDDR 3 memory(512Mb) 136 Ball BGA package
11 - Reserved



A1A:change video capture
enable setting

M56-P Strap

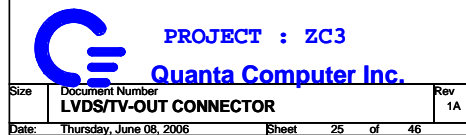
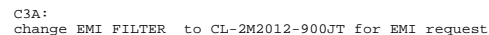
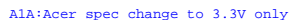
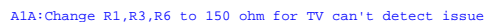
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M56X,M56P: INSTALL WITH ATT R5450,R5450,R5450, RC410,R5452 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M56X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM.MEM.AP.SIZE=0(128MB) 001x - No ROM.MEM.AP.SIZE=0(128MB) 010x - No Rom.MEM.AP.SIZE=0(64MB) 011x - No ROM.MEM.AP.SIZE=1(Reserved) 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NK25F01B ROM (ISSI), chip IDs from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0 - Slave VIP host port device present. 1 - No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

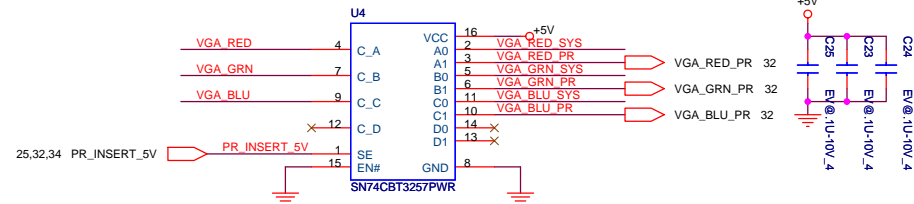
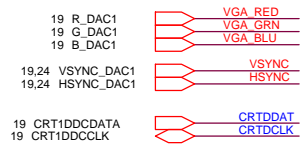
Board Straps

REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYP(1:0)	DVPDATA(1:0)	MEMORY TYPE AND SIZE SELECT->DVPDATA(1:0) 00 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 01 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Hynix GDDR 3 memory(512Mb) 136 Ball BGA package 11 - Reserved	00
DC_Strip1	GPIO(10)	Internal TMS Enabled 0 - Disabled 1 - Enabled	1
DC_Strip2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	1
DC_Strip3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Not detected	1
DC_Strip4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1

MEMORY TYPE AND SPEED SELECT



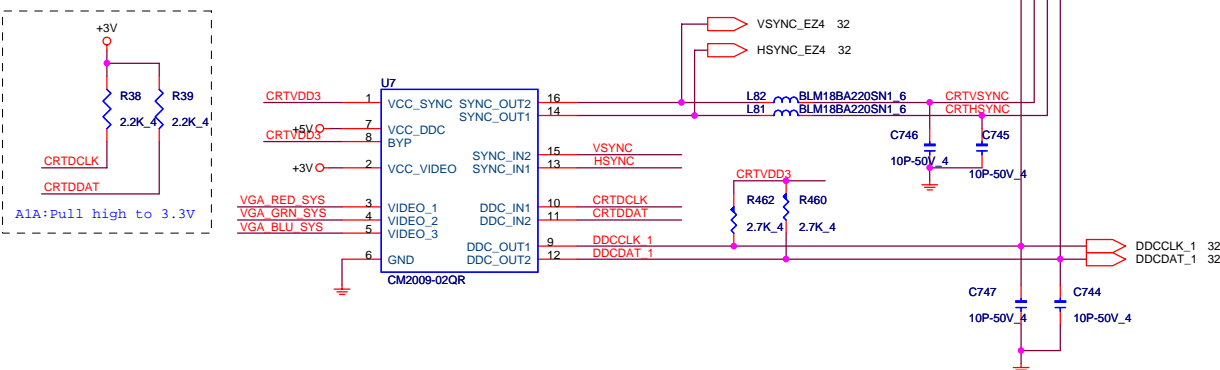
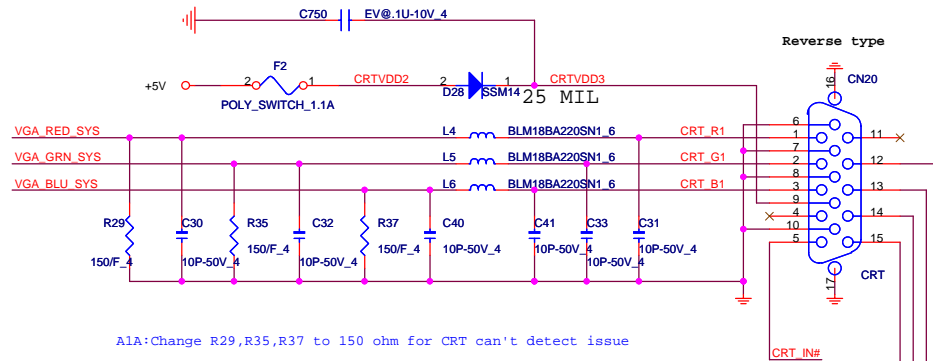
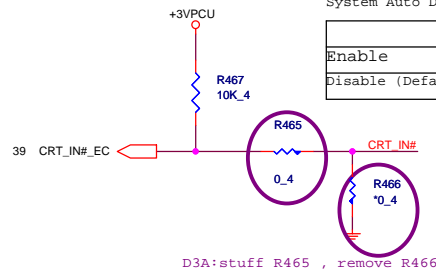


A1A:Change to SN74CBT3257PWR (Vin 5V)

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

System Auto Detect External CRT Device

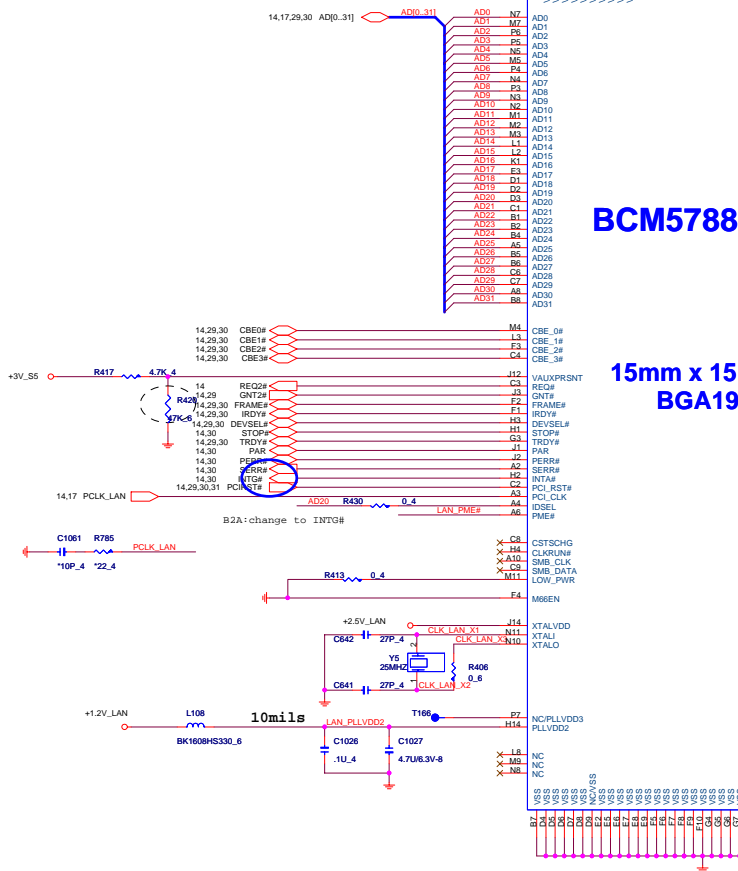
	R7059	R7058	R27
Enable	Not stuffed	Stuffed	Stuffed
Disable (Default)	Stuffed	Not stuffed	Stuffed

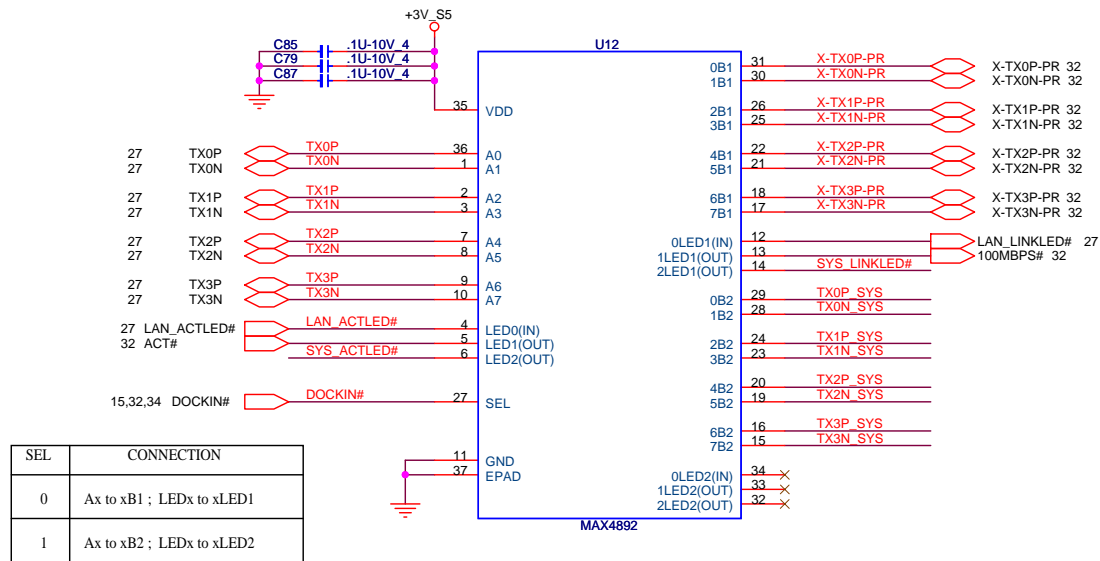


PROJECT : ZC3
Quanta Computer Inc.

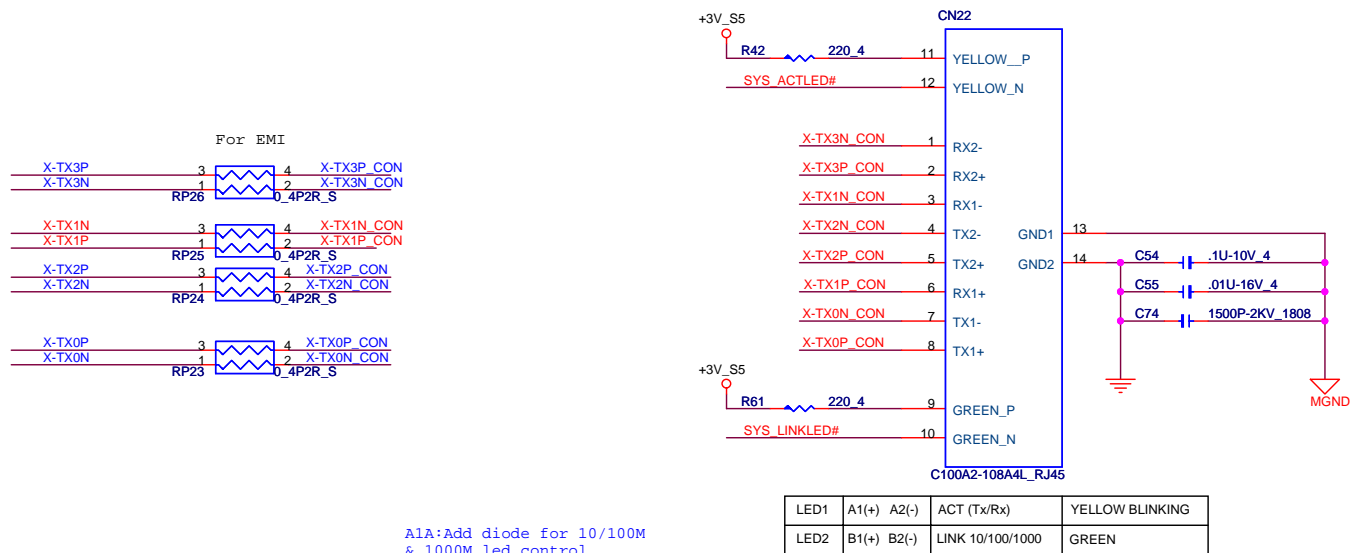
Voltage Rail	BCM5788MG
VDDIO_PCI	+3V3RUN(PCI SW)
2.5V_LAN	2.5V
1.2V_LAN	1.2V

LAN
BCM5787MKFBG :
AD20 REQ2#
GNT2# INTF#

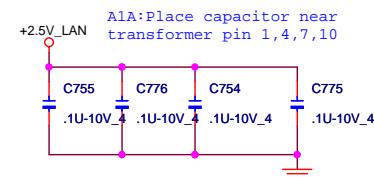




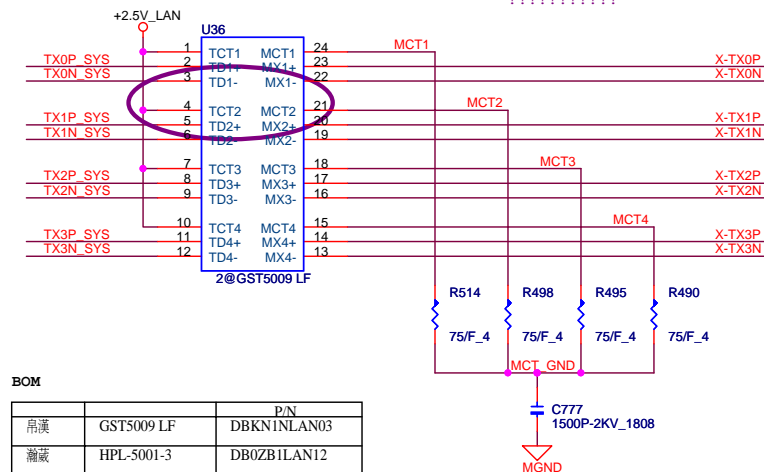
A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



A1A:Add diode for 10/100M & 1000M led control



D3A:change transformer to meet IEEE test, update to ???????????



BOM

品名	規格	P/N
吊環	GST5009 LF	DBKN1NLAN03
離散	HPL-5001-3	DB0ZB1LAN12

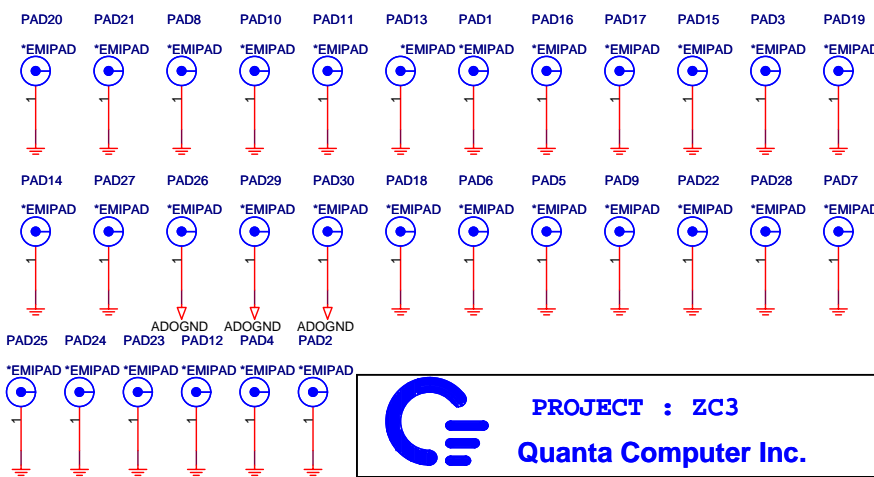
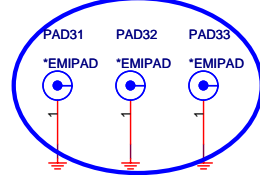
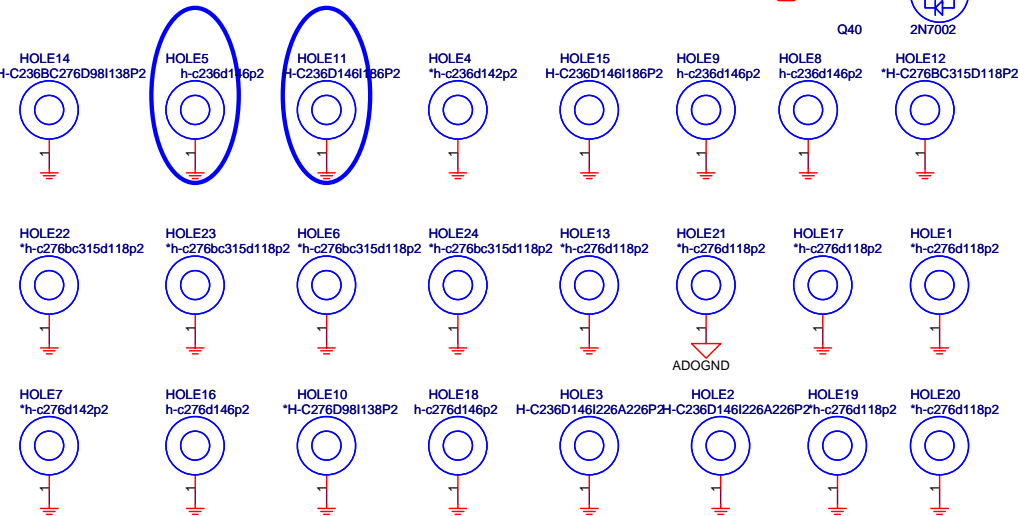
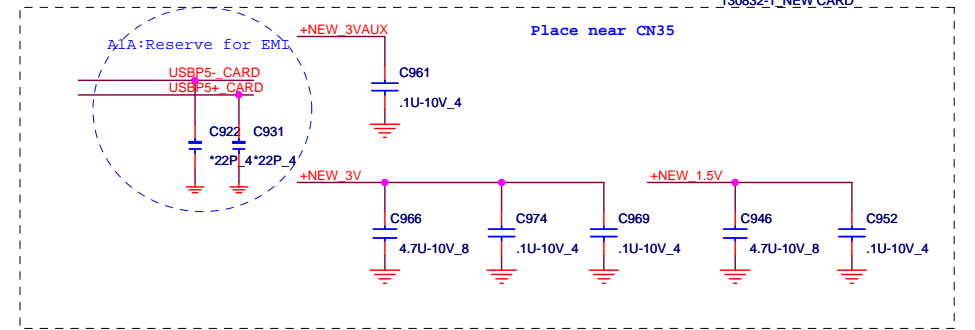
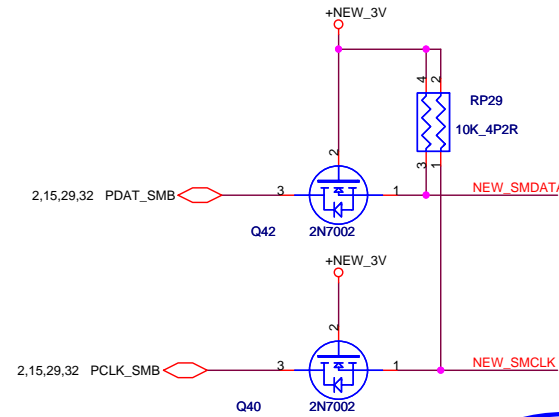
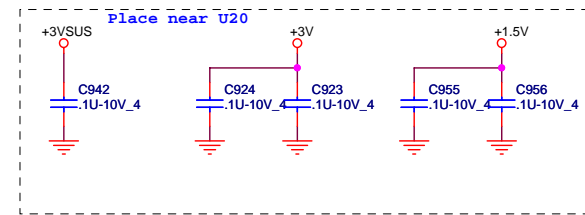
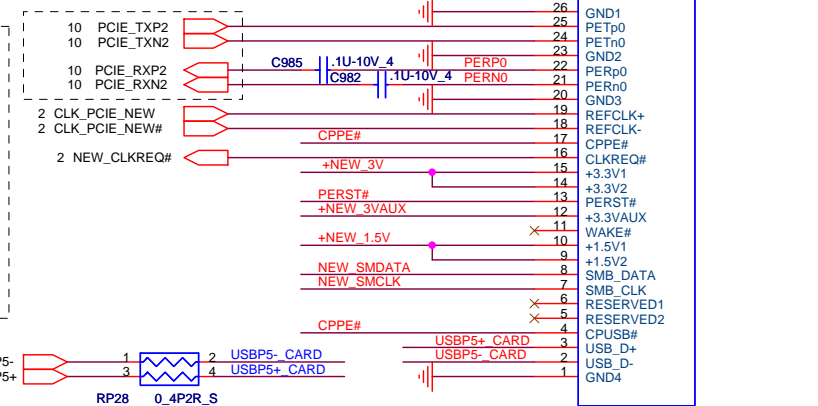
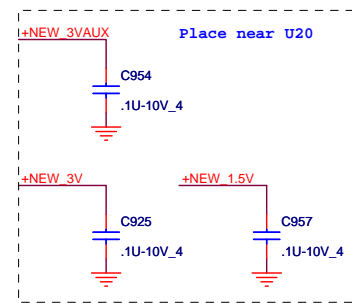
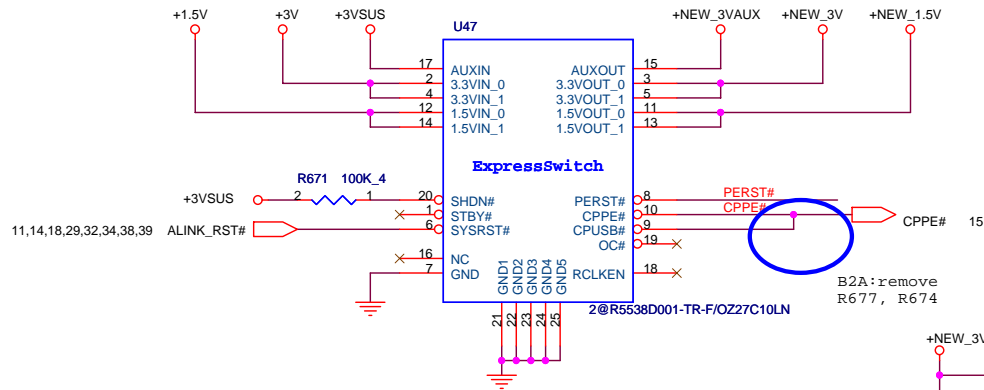
PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	TRANSFORMER/RJ45	1A
Date:	Thursday, June 08, 2006	Sheet 28 of 46

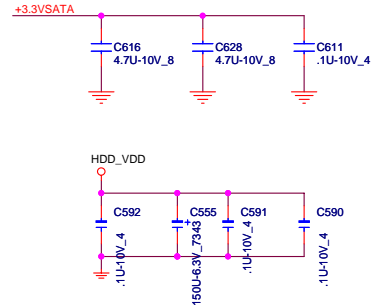
+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

A1A:Change New card power sw to Oz27c10

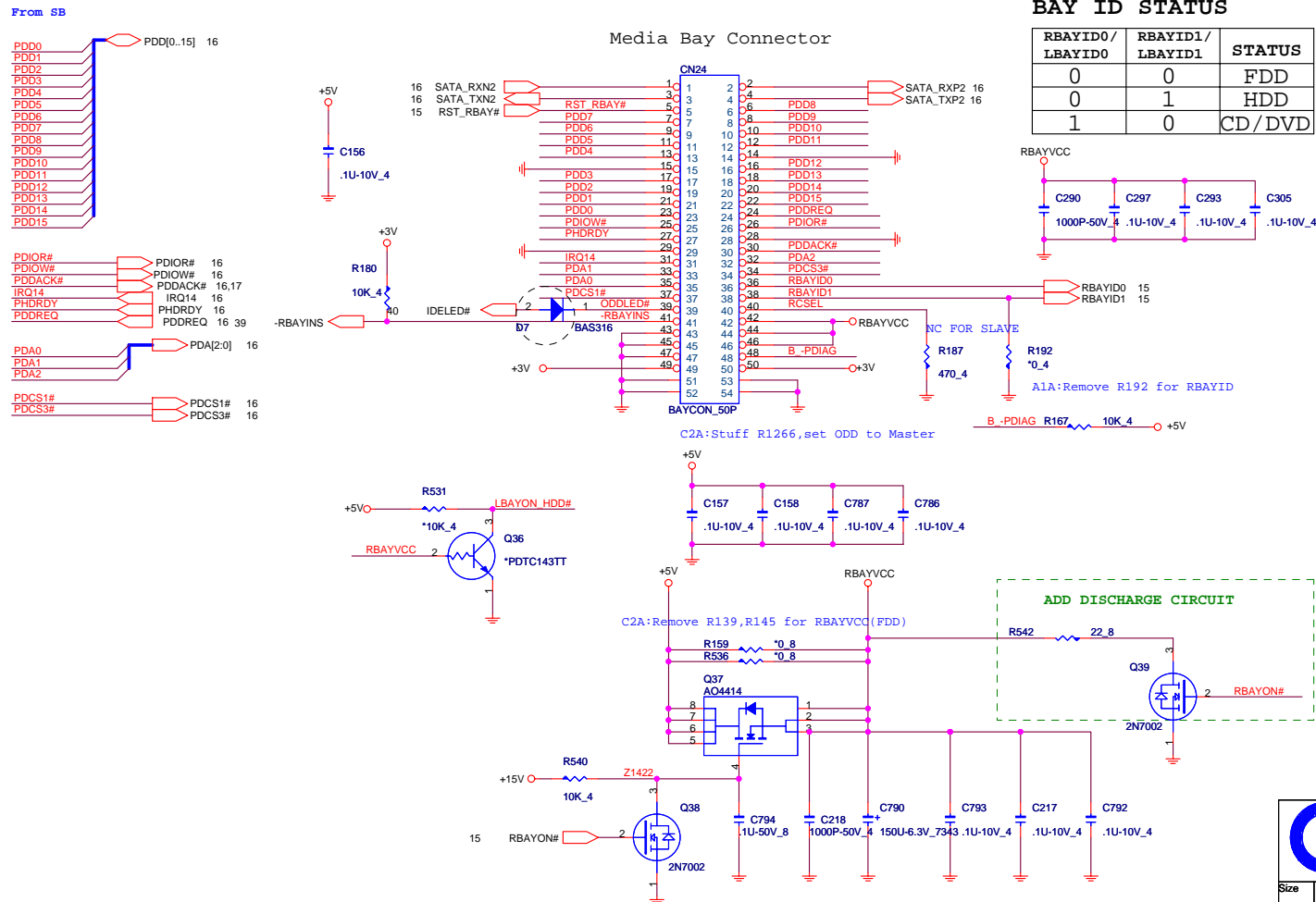
A1A:Change New card to small type(130832-1)
Reverse

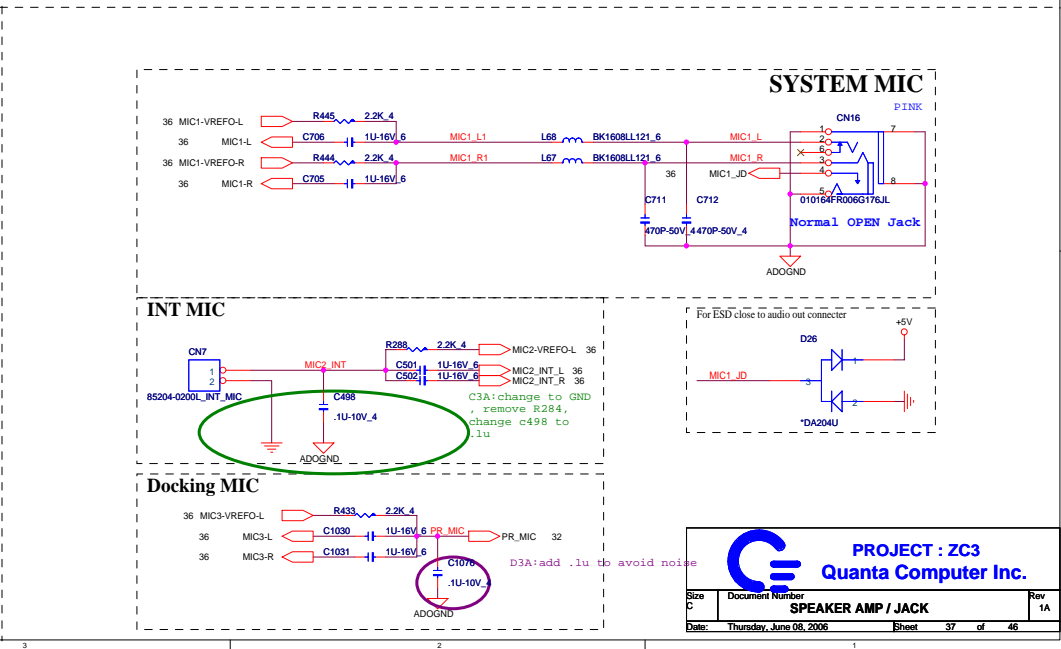
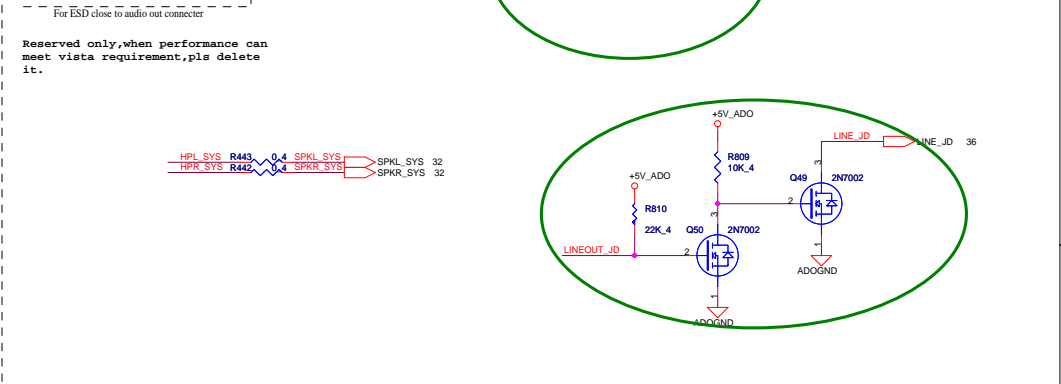
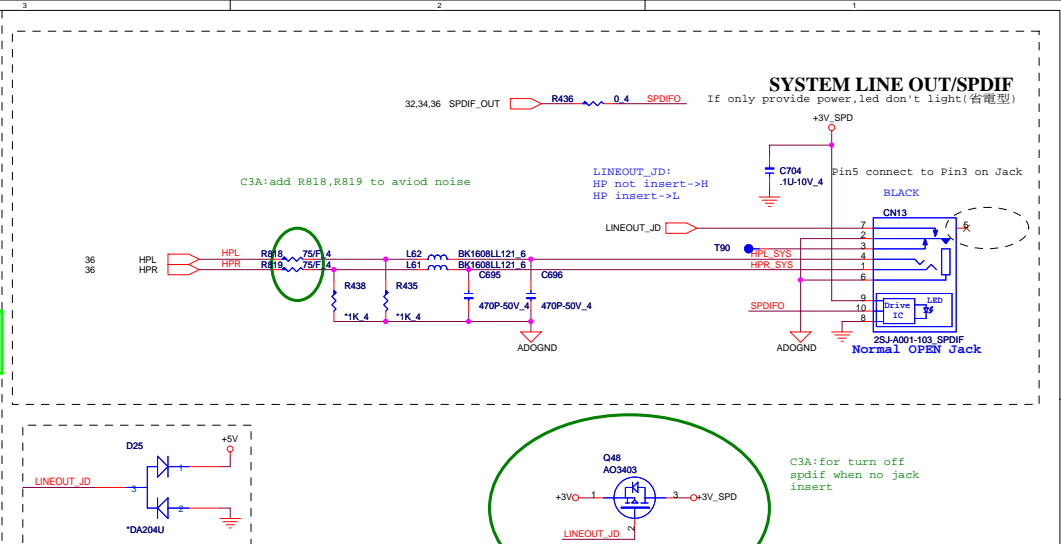


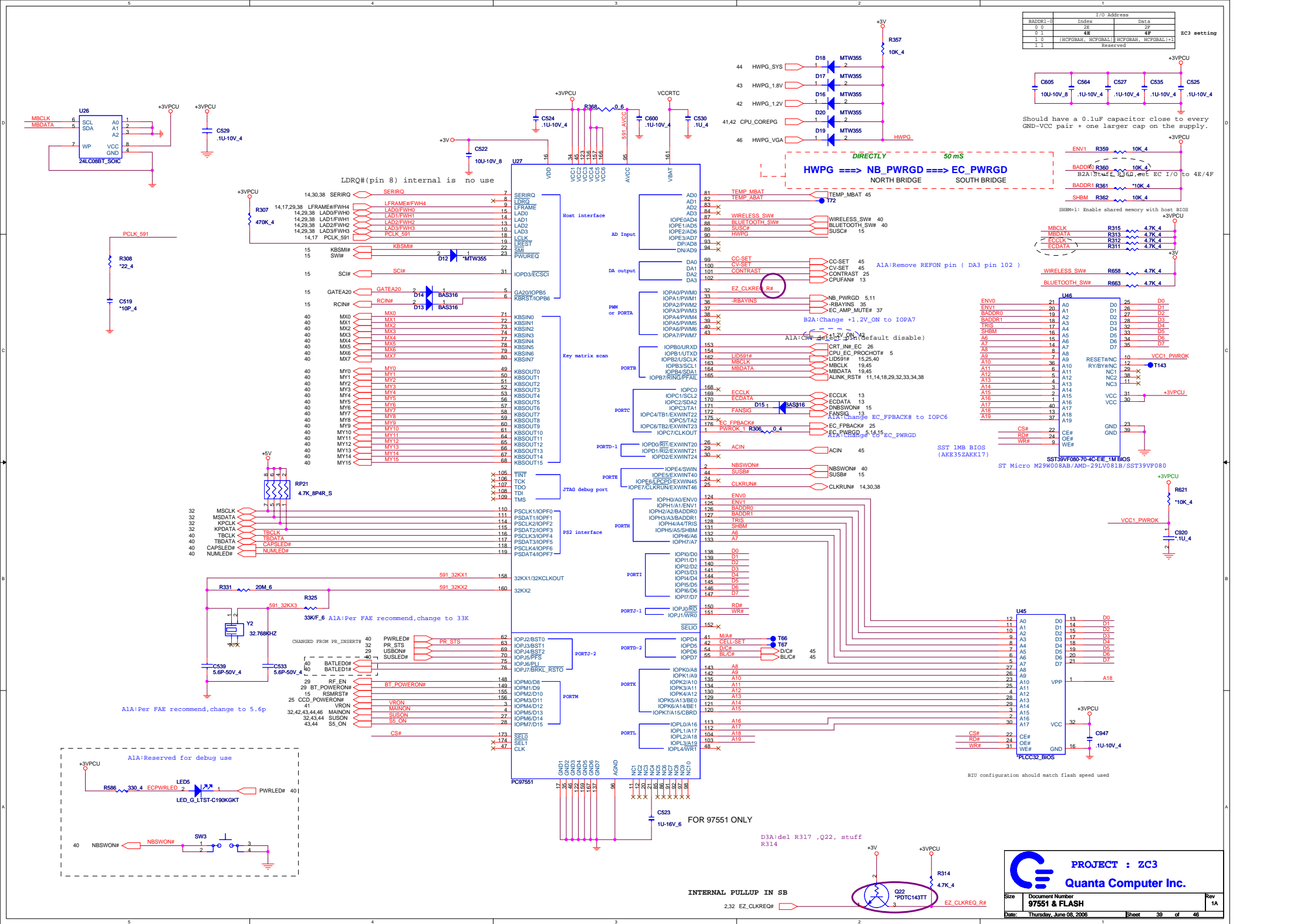
0654-122A4-L Serial ATA

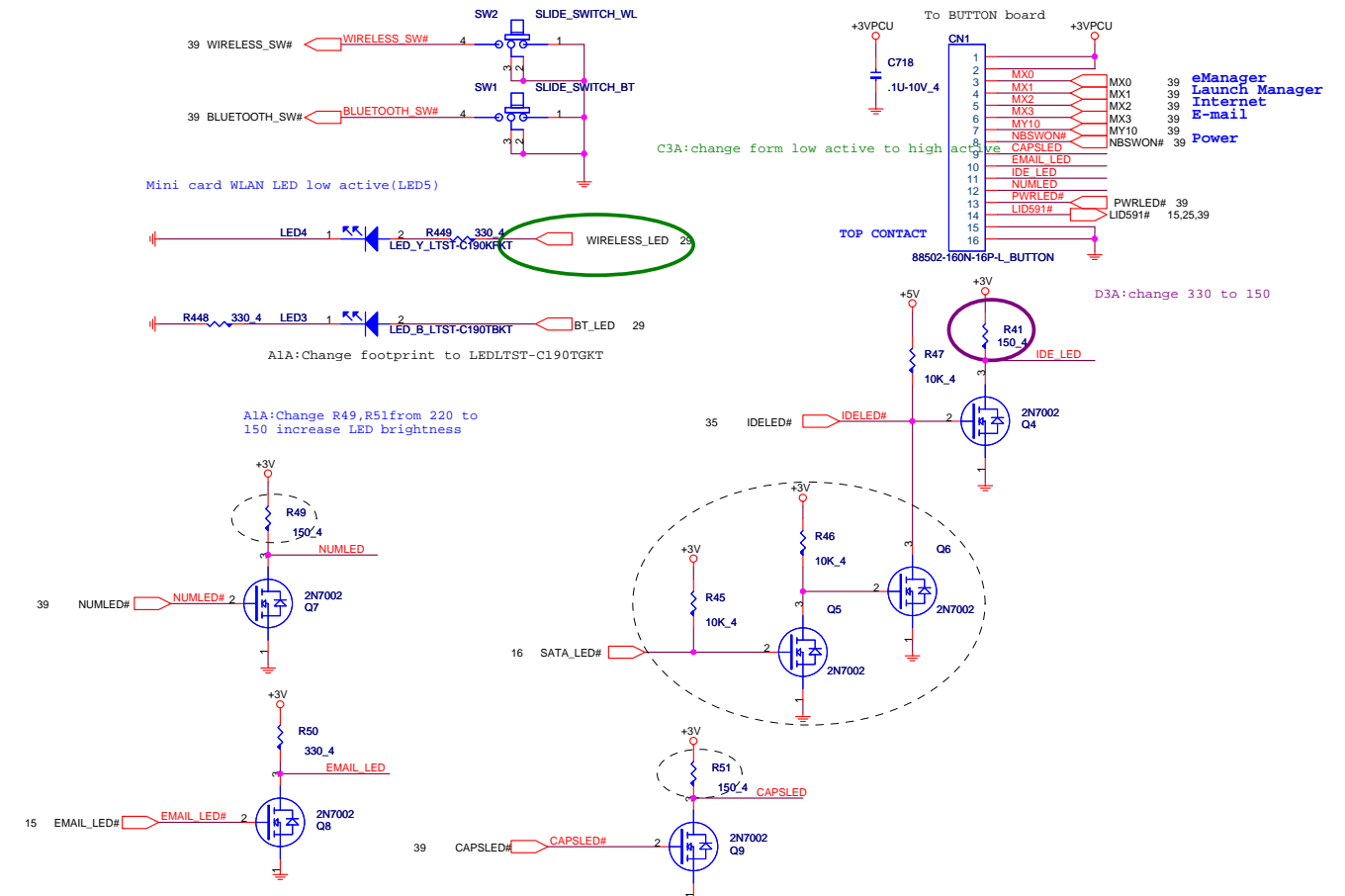
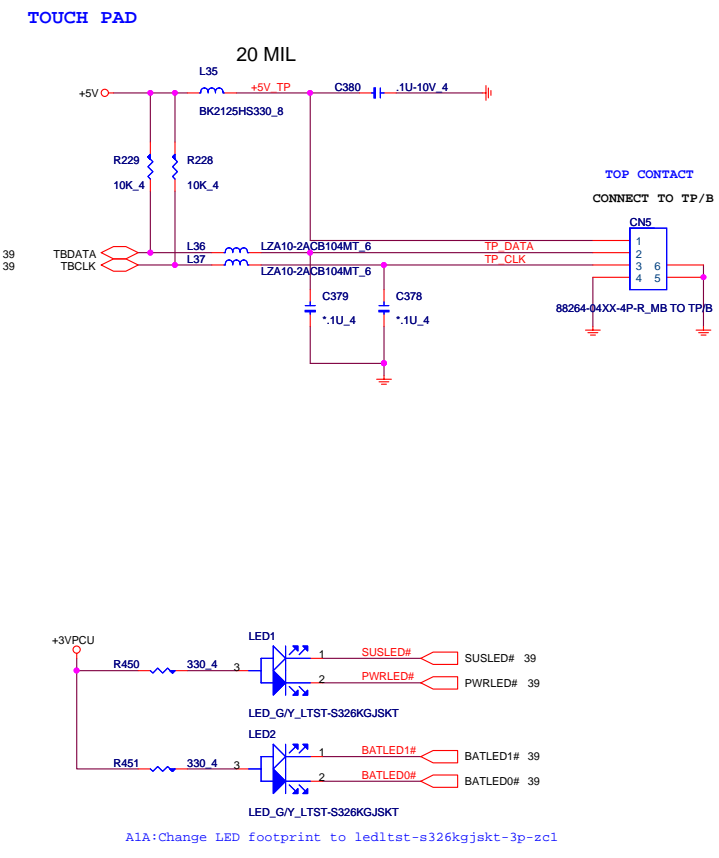
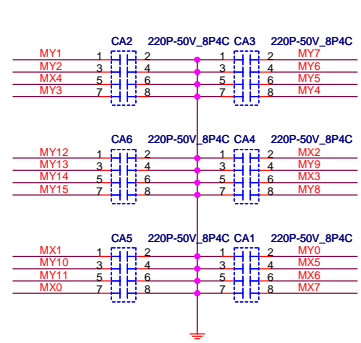
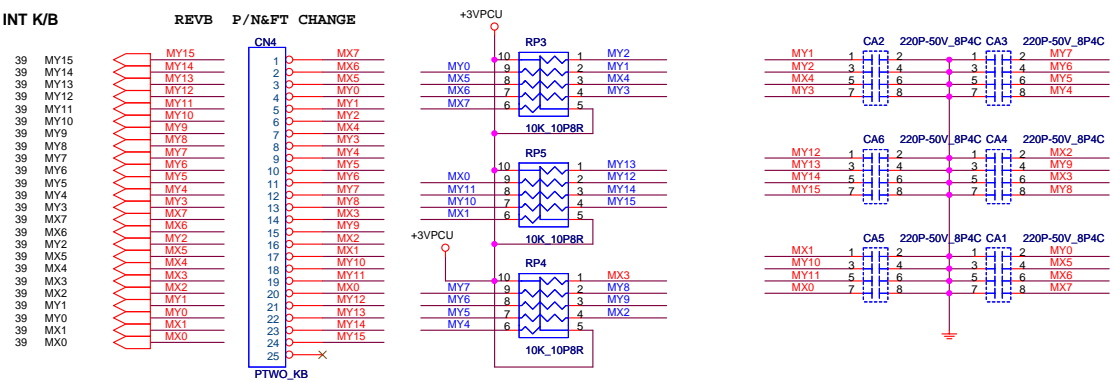


RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD

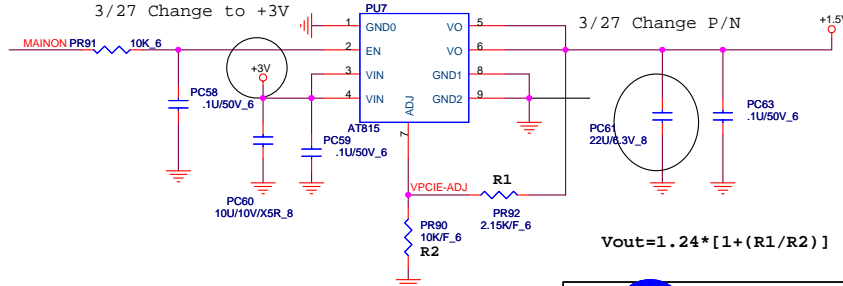
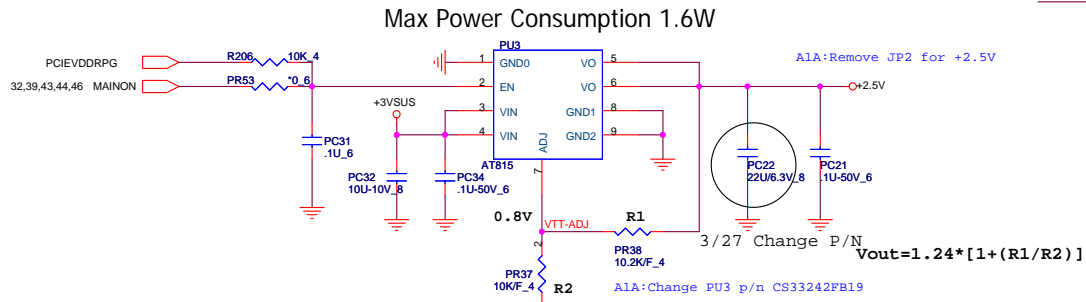
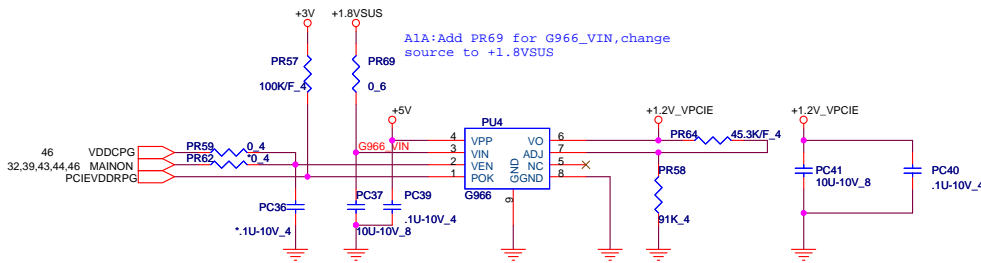
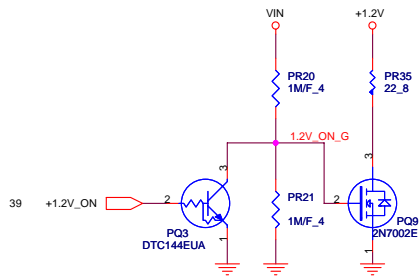
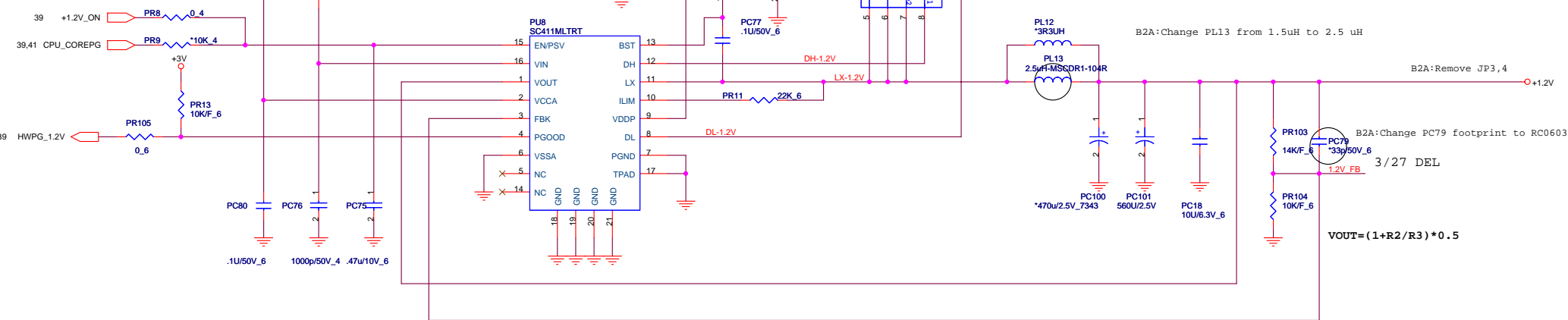


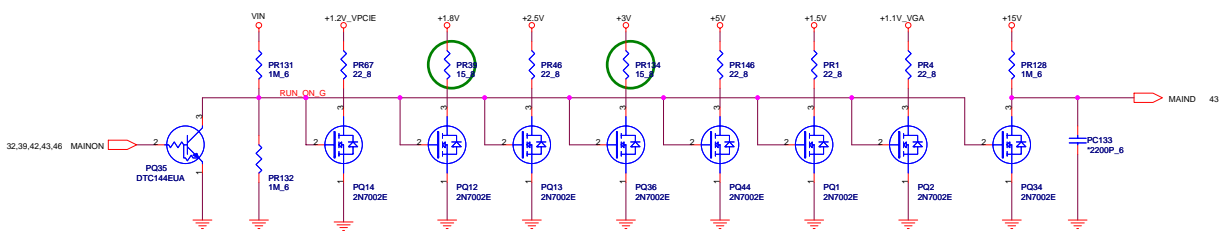
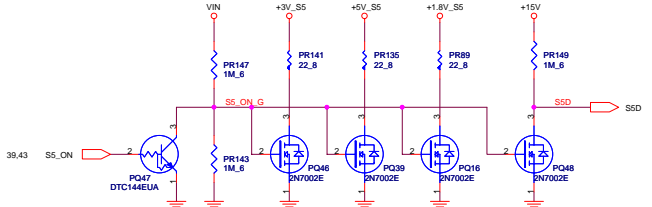
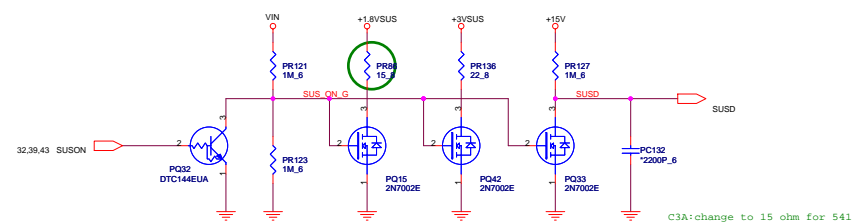
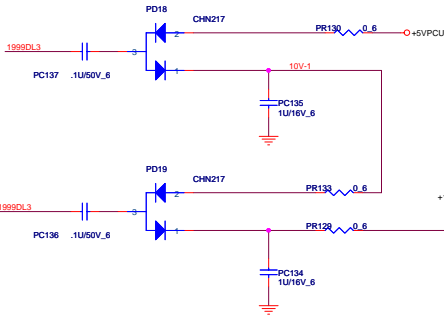
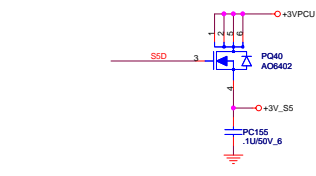
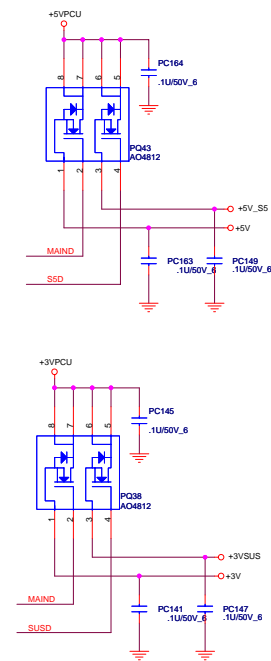
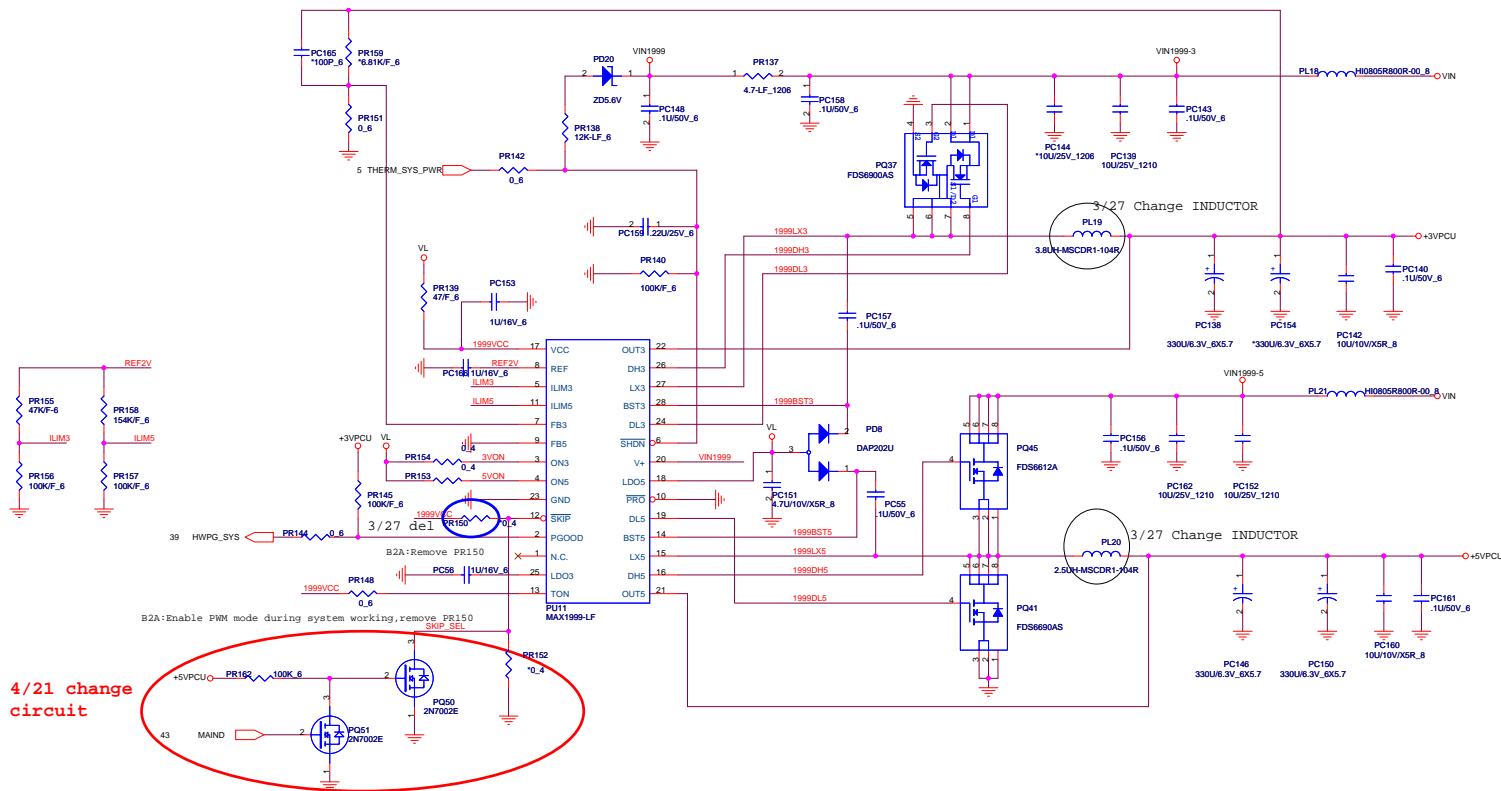






AMD power sequence:
VDDIO (+1.8VSUS), VTT (+0.9V_VTER), VDD
(CPU core power), and VLDI (+1.2V)





ALA:Change PJ1 footprint to 4 pin

D3A:change from BCPL1040218 to BCSBM104219 (EOL issue)

